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Development of a thermoelectric energy harvester with thermal isolation cavity by standard CMOS process

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ABSTRACT

A micro thermoelectric generator that combines the conventional in-plane and cross-plane designs is developed to harvest effectively the thermal gradient, where heat flux from the top to bottom surface is confined passing through the in-plane thermocouples. A thermal isolation cavity is created underneath the thermocouples to prevent heat loss, maintain temperature gradient, and improve output power. Analysis shows that, with 10 μm cavity depth, the thermocouple's temperature gradient is above 99% of the hot/cold side temperature difference. By comparison, it is only 14% for those without the isolation cavity. Simulation results show that the optimal thermocouple of 71 μm × 4 μm × 0.275/0.18 μm (length × width × thickness for P-/N-thermolegs) has matching electrical/thermal resistance and can achieve the maximum power factor 0.0473 μW/cm^2 K^2 and voltage factor 2.788 V/cm^2 K. The design is validated by standard CMOS process, where the isolation cavity is realized by dry etching post-process. Design verification by TSMC 0.35 μm 2P4M (2-poly and 4-metal) CMOS process shows that the thermocouple 60 μm × 4 μm can provide the power factor 0.0417 μW/cm^2 K^2 and voltage factor 2.417 V/cm^2 K.

1. Introduction

Recent studies on wireless sensor network aim at pervasive computing, ambient intelligence, and wearable electronics, in which small sensor and with sufficient power supply is required. Among all kinds of energy harvesters, micro thermoelectric generator (μTEG) converting waste heat into electrical power is promising for on-chip power supply. The first application was introduced to drive a wrist watch using a person's body heat [1]. Most developments since then have usually been produced by electrochemical deposition [2,3] of thermoelectric materials in V–VI compounds [4], but such thick-film process is often time-consuming. Thin-film process by using $(Bi_{0.25}Sb_{0.75})_2Te_3$ and $Bi_2(Se_{0.1}Te_{0.9})_3$ has been considered [5], but the materials are incompatible to CMOS process because of the contamination and process tool concerns.

Thermoelectric sensors have been successfully developed by CMOS process [6], where the silicon-based designs have the advantage of using thin-film process in semiconductor infrastructure for batch production. A μTEG design of 500 μm × 7 μm (length × width) Al/Si thermocouples was developed [7], but the membrane configuration of parallel thermal flow is impractical for on-chip thermal harvesting, as one would prefer thermally contacting the hot/cold sides on the top/bottom surfaces. Another design using polycrystalline silicon and silicon germanium (SiGe) was developed to deliver 0.112 μW at 5 K temperature difference [8], but the additional etching process may jeopardize the process stability. A thermoelectric generator using poly-SiGe was also applied to achieve about 1–2 μW on the watch-size area at 10–15 K temperature difference [14]. Another using poly-Si thermocouples to generate 0.00137 μW/cm^2 K^2 [10] and a modular design using Al/ploy-Si to deliever 0.00363 μW/cm^2 K^2 [11] have recently been reported; however, the above works using wafer-bonding are often low-yield and unsuitable for batch production. As most harvesters are difficult or incompatible to CMOS process due to material and process issues, a better design is needed.

2. Thermal isolation cavity design in CMOS process

A thermoelectric generator is composed of a large number of thermocouples connected thermally in parallel and electrically in series to achieve better conversion of temperature gradient into voltage. Heavily doped semiconductors as thermocouples have been proposed to replace metals due to their much higher thermoelectric power. Conventional thick-film design of cross-plane type converts energy from the heat passing across the chip plane. Some attempts have been made by thin-film process, but the output

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Nomenclature

A	area
d	depth of thermal isolative cavity
I	electrical current
k	thermal conductivity
K	thermal resistance
L	length of thermocouple
N	number of thermocouple
P_{out}	specific power
Q	thermal flow
R	electrical resistance
S	seebeck coefficient
t	thickness
T	temperature
U	open-circuit voltage
W	width of thermocouple

Greek letters

ϕ_p	power factor
ϕ_u	voltage factor

Subscripts

c	of cold side
g	of thermocouple
h	of hot side
n	of N-thermoleg
p	of P-thermoleg
int	of interface

power remains very low because of the extreme short thermocouples (<1 μm). The in-plane design converts energy from the heat passing within the chip plane [12], but the output power is drastically decreased by the heat dissipation through the substrate. A design using thermal isolation cavity beneath the thermocouples [8,11] to minimize heat leakage as shown in Fig. 1(a) is employed in this work, across which the heat input from the top surface is confined passing through the in-plane thermolegs to facilitate better thermoelectric conversion.

For a thermocouple with hot and cold junction temperature T_h and T_c, the temperature difference $\Delta T_g = T_h - T_c$ generates an open-circuit voltage U_o, $U_o = S\Delta T_g$, where $S = S_p - S_n$ is the combined Seebeck coefficient. The temperature gradient $\Delta\hat{T}_g = \Delta T_g/\Delta T$, defined by the ratio of ΔT_g over the hot/cold side temperature difference $\Delta T = T_1 - T_0$, is to characterize the effectiveness of thermal isolation cavity in μTEG. Fig. 1(b) illustrates three thermocouples interconnected by the metal pads. A single thermocouple shown in Fig. 1(c) denotes the length, width, and thickness of a thermoleg by L_g, W_g, and t_g, and A_h and A_c are the contact area of the hot and cold junctions, respectively, and d is the cavity depth. Finite element simulations (ANSYS® 9.0) have been applied to evaluate the effectiveness of thermal isolation design. The model is by quadrilateral 2D element (PLANE55) on a single thermoleg, and the boundary condition is set at 20 K temperature difference between the nodes on the top and the bottom surfaces. The material properties are k_p = 31.2 W/m K, k_n = 31.5 W/m K, the thermal conductivity of oxide on the hot side (thickness 0.29 μm) k_i = 1.1 W/m K, and that of the Si substrate on the cold side (thickness 650 μm) k_c = 168 W/m K. The temperature profile of a typical thermoleg with and without the isolation cavity are shown in Fig. 2(a), in which the heat flow is confined in the thermoleg with thermal isolation, but there is only small temperature gradient across the thermoleg without thermal isolation because of heat leakage through the silicon substrate. The simulation shows that $\Delta\hat{T}_g > 99\%$ can be achieved by 10 μm cavity depth. By comparison, there is only 14% for the thermoleg without thermal isolation. Fig. 2(b) shows the temperature gradient of a thermocouple with 2–10 μm cavity depth, where it remains above 99% for all upto 120 μm in length and the heat flow is confined within the thermolegs. The simulation is based on a thermoleg model with only one metal layer. In practice, a thermoelectric generator chip may have more than one metal layer and many metal via layers, but the simulations in Fig. 2 are valid on the model with more thermal conductive metal layers.

3. Performance of the generator with thermal isolation

The above analysis illustrates that heat leakage becomes negligible on the thermolegs with 10 μm thermal isolation cavity, and the generator performance can thus be calculated by the model in Strasser et al. [8] assuming no heat loss. In a generator with N thermocouples, the thermal resistance of the hot side, thermolegs, and cold side can be modeled by a thermal circuit represented by K_h, K_g, and K_c, respectively, as illustrated in Fig. 1(a). Previous works have been plagued by undesirable Joule heating from relative large Ohmic resistance and by negligible temperature gradient across the thermolegs from small thermal resistance. Optimal design of the thermoleg geometry for higher output power, voltage, and current is thus necessary. The thermal resistance are determined by the thermoleg geometry,

$$K_h = \frac{1}{2N}\frac{t_h}{k_h A_h} + K_{int} \tag{1a}$$

$$K_g = \frac{1}{N}\left(\frac{L_p}{k_p W_p t_p} + \frac{L_n}{k_n W_n t_n}\right) \tag{1b}$$

$$K_c = \frac{1}{2N}\frac{t_c}{k_c A_c} \tag{1c}$$

where L, W, t, A, K and k is length, width, thickness, area, thermal resistance, and thermal conductivity, and the subscripts p, n, g, h, c, and int refer to P-thermoleg, N-thermoleg, thermoelectric couple, hot side, cold side, and interface, respectively. Note that the precise estimation of K_{int} is difficult. The metal–ceramic interface (1–20 cm^2 K/W) is assumed in the simulations [13] and it is later validated experimentally at about 9 cm^2 K/W.

In addition to the thermal resistance, the electrical resistance

$$R_g = N\left(\rho_p\frac{L_p}{W_p t_p} + \rho_n\frac{L_n}{W_n t_n}\right) \tag{1d}$$

is as critical to device mininaturation, where ρ is the electrical resistivity. The output power is

$$P_{out} = \frac{N^2 S^2}{4R_g}(\Delta T_g)^2. \tag{2}$$

at matching electrical resistance load. By the thermal model, the operation condition ΔT can be represented by

$$\Delta T = \Delta T_g + K_h Q_h + K_c Q_c, \tag{3}$$

where Q_h and Q_c are the thermal flow on the hot and cold sides, respectively, and both can be calculated by the thermal balance and the Joule heat at the junctions. The power factor and voltage factor, $\phi_p = \frac{P_{out}}{A\Delta T^2}$ and $\phi_u = \frac{U_0}{A\Delta T}$, have been employed to evaluate the generator performance [8–11,14]. In view of the effectiveness of the thermal isolation cavity as illustrated in Fig. 2, the power factor and voltage factor of the thermocouple are similar to those in Strasser et al. [8],

$$\phi_p = \frac{R_g}{4A\Delta T^2 N^2 S^2}\left[\frac{1}{K_c} - \frac{1}{K_h} + 2C_2\cos\left(\frac{1}{3}\arccos\left(\frac{C_1}{C_2^3}\right) + \frac{4\pi}{3}\right)\right]^2 \tag{4}$$

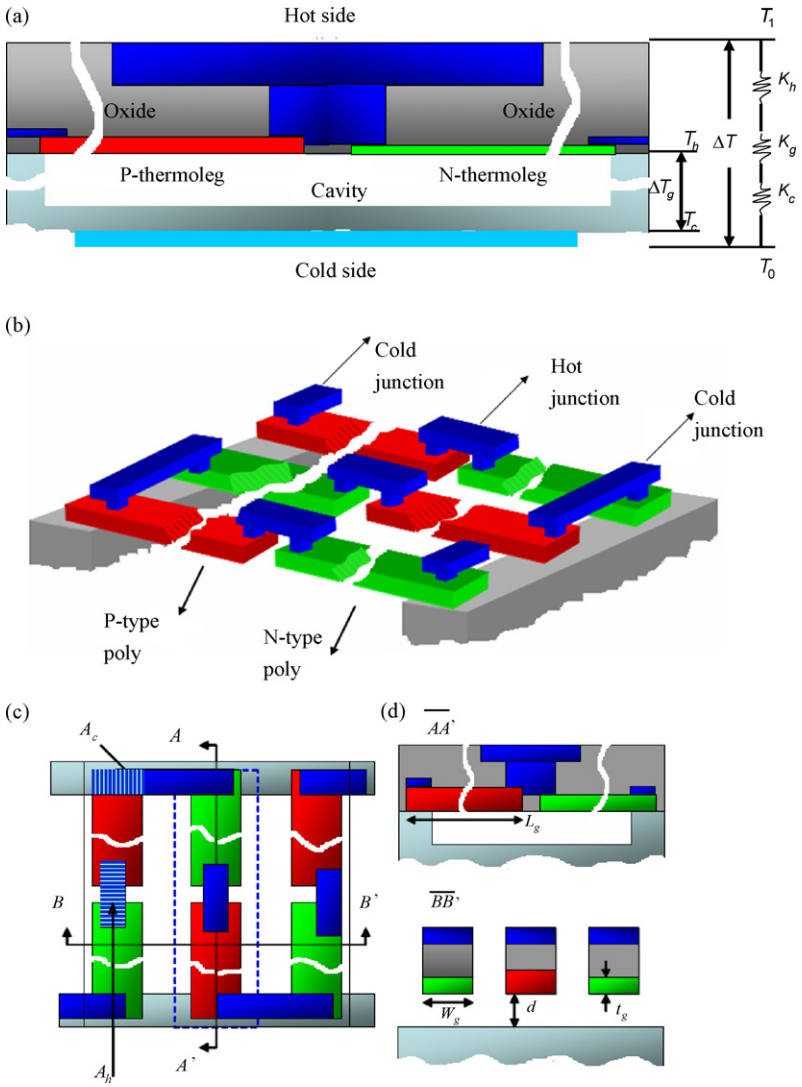

Fig. 1. (a) The thermal model of the μTEG, (b) the schematic diagram of the μTEG with thermal isolation cavity, (c) the top view, and (d) the cross sections.

and the voltage factor ϕ_u as

$$\phi_u = \frac{R_g}{A\Delta TN\,S}\left[\frac{1}{K_c} - \frac{1}{K_h} + 2C_2\cos\left(\frac{1}{3}\arccos\left(\frac{C_1}{C_2^3}\right) + \frac{4\pi}{3}\right)\right]. \quad (5)$$

where A is the area of the generator and

$$C_1 = \left(\frac{1}{K_c} - \frac{1}{K_h}\right)\left(\frac{1}{K_c^2} + \frac{2}{K_cK_h} + \frac{1}{K_h^2} + \frac{4}{K_gK_h} + \frac{4}{K_gK_c}\right) + 2\frac{N^2S^2}{R_g}\left(\frac{T_0}{K_c^2} - \frac{T_1 - T_0}{K_cK_h} - \frac{T_1}{K_h^2}\right) \quad (6a)$$

and

$$C_2 = \sqrt{\frac{1}{K_c^2} + \frac{2}{3K_cK_h} + \frac{1}{K_h^2} + \frac{8}{3K_g}\left(\frac{1}{K_c} + \frac{1}{K_h}\right) + \frac{4}{3}\frac{N^2S^2}{R_g}\left(\frac{T_0}{K_c} + \frac{T_1}{K_h}\right)}. \quad (6b)$$

TSMC 0.35 μm CMOS process with two poly-silicon layers and four metal layers (2P4M) is employed in analysis and design verification. This standard mixed-signal CMOS process is for integration of digital, analog circuit and SoC (system-of-chip) design. Though the component geometry in IC design is different from that used in thermoelectric generator deign, the data of thermoelectric material properties from standard CMOS process qualification are adopted in this work. Consider symmetric design with $L_p = L_n = L_g$, $L_g = 1$–150 μm, and $W_p = W_n = W_g$, $W_g = 1$–10 μm, $t_p = 0.275$ μm, $t_n = 0.180$ μm, the oxide thickness $t_h = 0.29$ μm on the hot side and the substrate thickness $t_c = 650$ μm on the cold side. The material properties of poly-silicon in standard CMOS process are: $S_p = 103$ μV/K, $S_n = -57$ μV/K, $\rho_p = 2.21$ μΩ m, $\rho_n = 0.813$ μΩ m. Fig. 3(a) illustrates the power factor calculated by Eq. (4) for the generator with $W_g = 4$ μm and 8 μm. The optimal design is $L_g^* = 71$ μm and $W_g = 4$ μm achieving the power factor 0.0473 μW/cm^2 K^2. Sim-

Table 1
Measured power and voltage factors of the μTEGs.

No.	$L_g \times W_g$ (μm)	U_{out} (mV)	I (μA)	ϕ_p (μW/cm^2 K^2)	ϕ_u (V/cm^2 K)
1	20 × 4	2.0	0.1	0.0021	0.590
2	30 × 4	3.9	0.2	0.0081	1.150
3	40 × 4	5.6	0.3	0.0175	1.703
4	60 × 4	7.2	0.4	0.0417	2.417
5	120 × 4	8.2	0.5	0.0300	2.212
6	20 × 8	2.1	0.2	0.0044	0.571
7	30 × 8	2.9	0.3	0.0091	0.986
8	40 × 8	3.8	0.4	0.0158	1.292
9	60 × 8	5.2	0.6	0.0325	1.768
10	120 × 8	5.5	0.7	0.0401	2.384

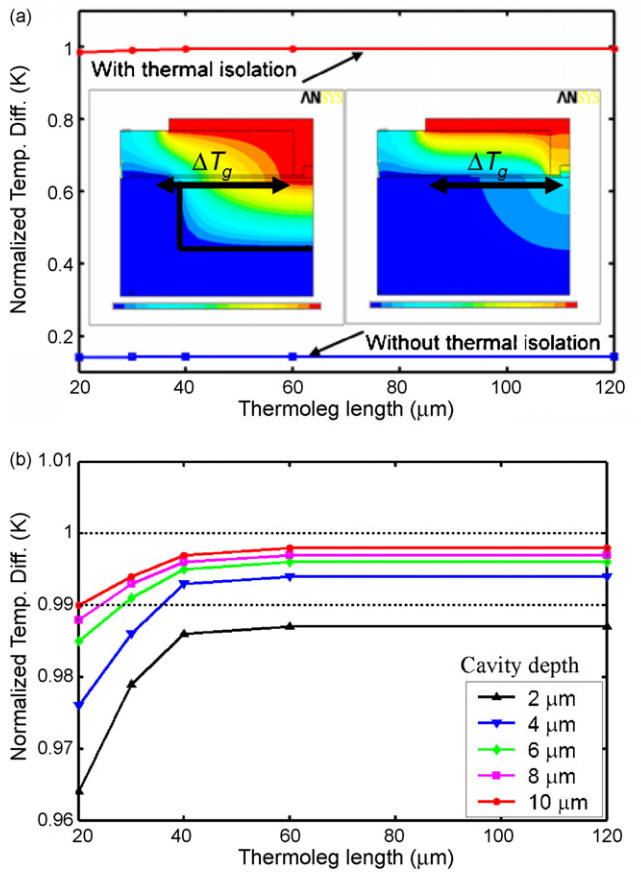

Fig. 2. (a) Numerical results of the temperature gradient with and without the thermal isolation design, and (b) the thermal isolation effectiveness at different cavity depths.

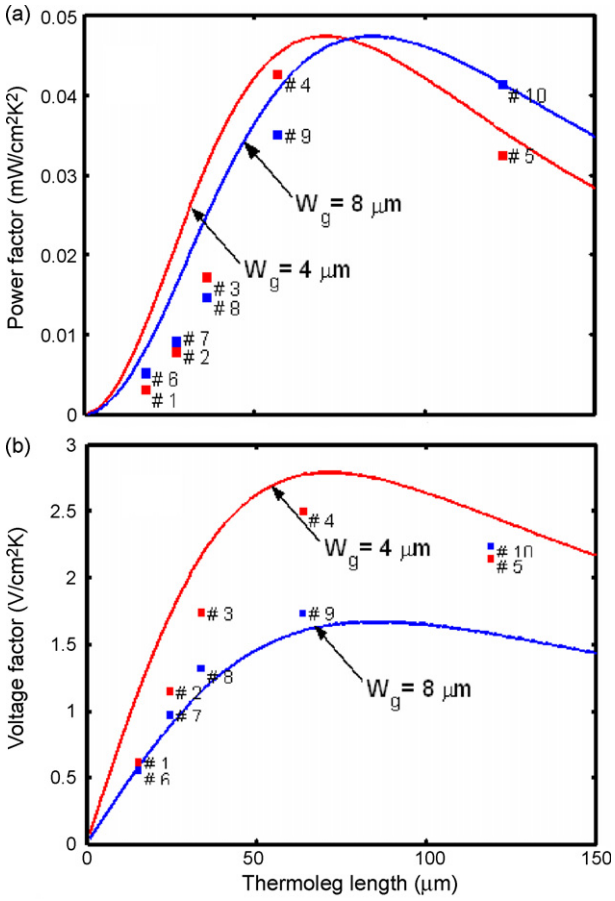

Fig. 3. (a) The power factor, and (b) the voltage factor of the generator at 1–150 μm thermoleg length and the optimal power factor is 71 μm × 4 μm or 85 μm × 8 μm. The measurement data of the generator are also labled.

ilarly $L_g^* = 85\ \mu m$ and $W_g = 8\ \mu m$ at the same power factor because longer L_g requires wider W_g for thermal resistance matching. The voltage factor ϕ_u is shown in Fig. 3(b), where the maximum is 2.788 V/cm^2 K at $L_g^* = 71\ \mu m$ and $W_g = 4\ \mu m$, and 1.669 V/cm^2 K at $L_g^* = 85\ \mu m$ and $W_g = 8\ \mu m$. The regions away from the maximums in Fig. 3(a) and (b) indicate resistance mismatching, from which either ΔT_g or Q_g is too low for thermoelectric conversion. This is also observed by the tempreature gradient and thermal flow through the thermocouples as shown in Fig. 4(a) and (b). The design of longer thermoleg, thus higher K_g, allows only small thermal flow, and conversely shorter thermoleg can only draw small temperature gradient across the junctions. Both render low voltage and power. For the example of a design with 10 μm × 4 μm × 0.18 μm ($L_g \times W_g \times t_g$), the thermocouple's thermal resistance from Eq. (1b) is 2.90×10^5 K/W. A 1 cm^2 μTEG with 238,100 thermocouples has only 1.216 K/W, and the thermal resistance is about the same as 1.555 K/W in Huesgen et al. [11] for the thermolegs of 120 μm × 40 μm × 0.7 μm (length × width × thickness). Thermal resistance in this range is much lower than the typical interface resistance K_{int} so that the mismatch will lead to small temperature gradient across the thermocouples. Advanced microchannel heat sink is required to bring down to $K_{int} = 0.05$ cm^2 K/W [13]. The thermal model in predicting the optimal size is a 1D model, and the electrical resistance and thermal resistance are assumed to be only a function of the geometric and material properties of the thermoleg in Eqs. 1(a)–1(d). Investigation of these thermoelectric properties remains needed.

4. Implementation by CMOS process

The cross section of TSMC 0.35 μm 2P4M CMOS process is shown in Fig. 5(a) with poly-silicon (Poly1 and 2), aluminum (M1–4), intermetal oxide (IMD1–4), gate oxide (GOX), field oxide (FOX), capacitor

Table 2
Comparison with CMOS-compatible μTEGs reported in the literature.

	CMOS integrated?	Thermoelectric materials	Power factor ϕ_p (μW/cm^2 K^2)	Voltage factor ϕ_u (V/cm^2 K)
[7]	No	Al/Si	0.091	–
[8]	Yes (modified)	Poly-Si	0.0426	2.6
		Poly-SiGe	0.0352	2.2
[9]	No	Poly-SiGe	0.00510	0.013 (Natural) 0.053 (Forced)
[10]	No	Al/poly-Si	0.00137	0.746
		BiTe	–	2.38
[11]	No	Al/poly-Si	0.00363	0.746
		BiTe	0.00814	2.38
This work	Yes	Poly-Si	0.0417	2.417

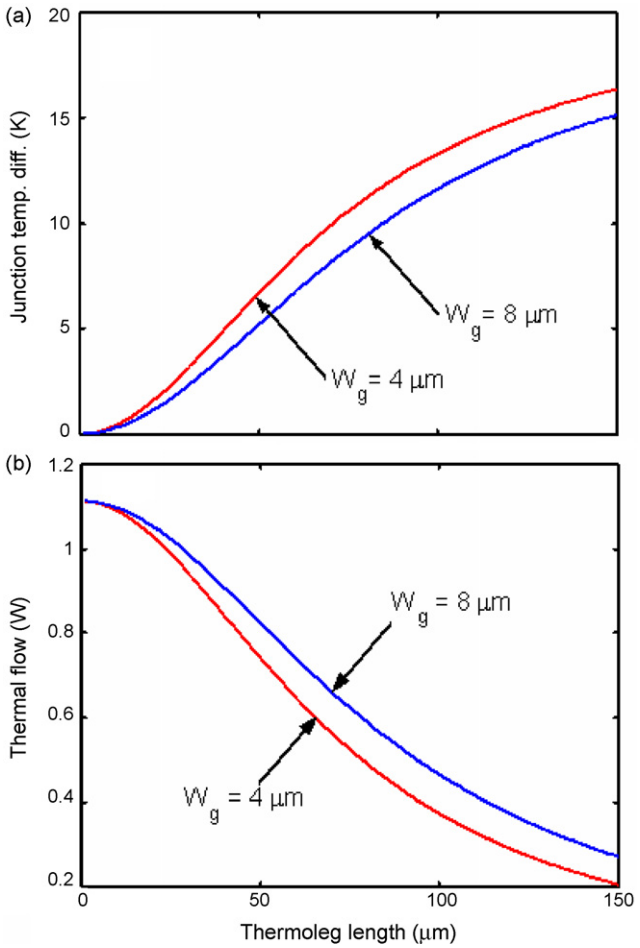

Fig. 4. (a) Hot/cold junction temperature difference, and (b) thermal flow through thermocouples in the generator.

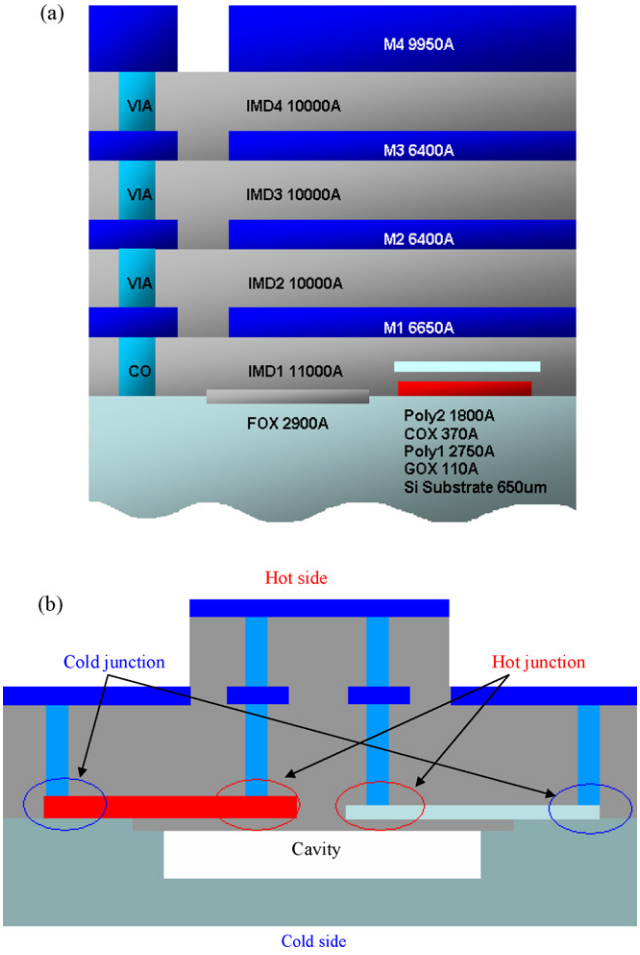

Fig. 5. (a) The cross section of the 0.35 μm 2P4M CMOS process, and (b) the schematic diagram of the generator.

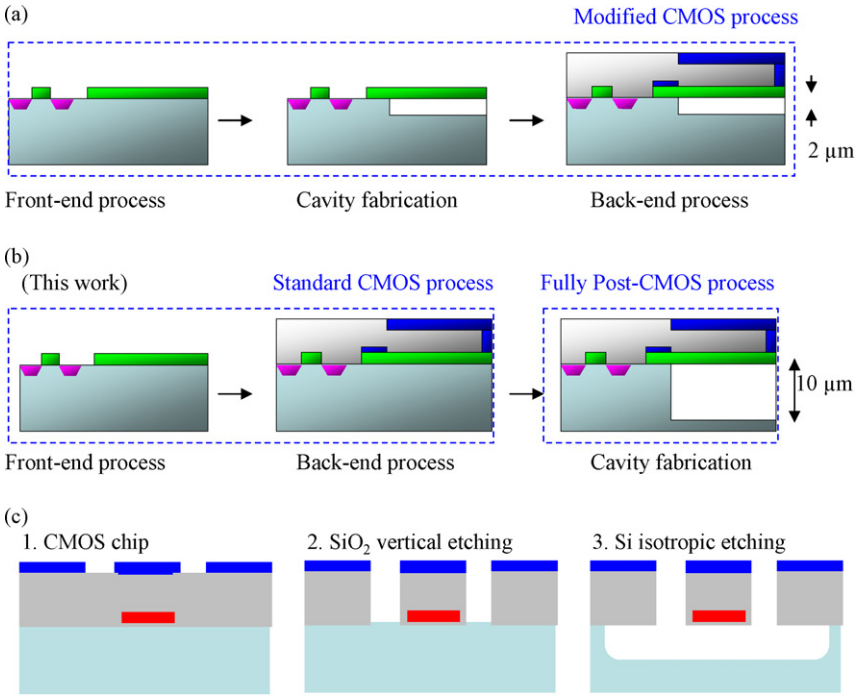

Fig. 6. Fabrication of the generator by (a) the modified CMOS process to have 2 μm cavity [8], (b) fully post-CMOS process in this work, where etching is conducted only after all thin-film depositions, and (c) post-CMOS process by SiO_2 vertical etching and Si isotropic etching to create the thermal isolation cavity.

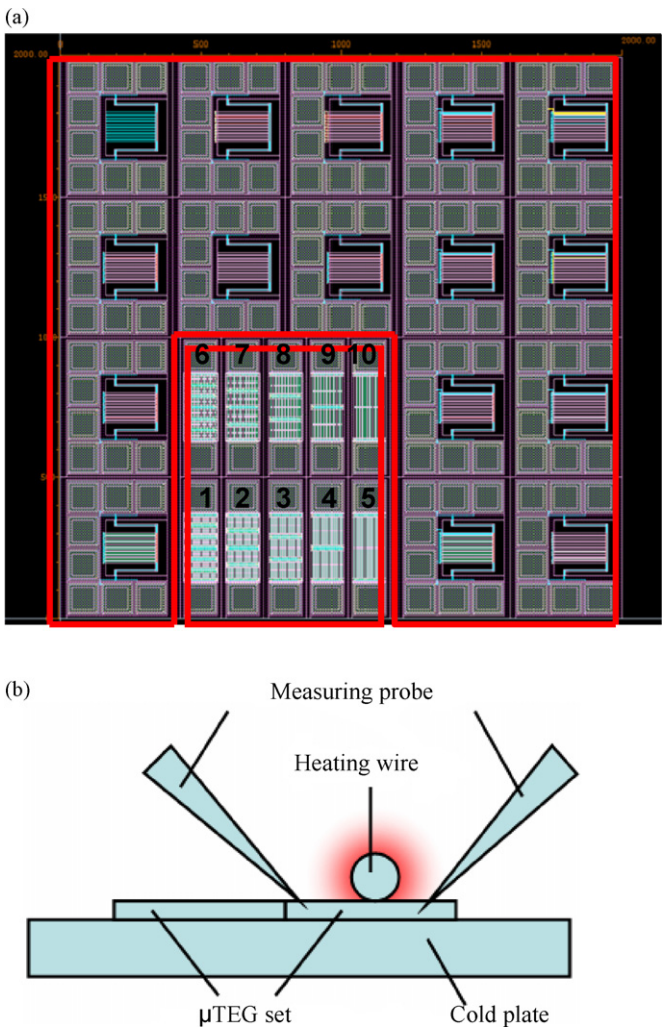

Fig. 7. (a) Photomicrograph of the2000 μm × 2000 μm chip with 10 μTEGs in the center and test structures around the perimeter, and (b) the experimental setup for measuring the generator performance.

oxide (COX), metal contact (CO), metal via (VIA1–3) layers in single crystallized silicon substrate. Fig. 1(c) illustrates that the patterned poly-silicon layers serve as the thermolegs and they are interconnected by the aluminum pads to form the hot/cold junctions on the oxide layer. Poly1 layer serves as the P-thermolegs and Poly2 layer as N-thermolegs. M1 layer serves as the interconnections of thermolegs, and M2, M3, and M4 layers as the thermal conductor at the hot junctions, and M3 and M4 layers also as the etching masks during post-process of creating the thermal isolation cavity. FOX layer serves as the protection of thermolegs during isotropic silicon etching, and CO and VIA1–3 layers as the interconnections of the layers. Fig. 5(b) illustrates the schematic of the CMOS thermoelectric generator.

The 10 μm thermal isolation cavity has been implemented to maintain the temperature gradient between the hot and cold junctions. Similar design has previously been proposed [8] by an additional etching between the front- and back-end processes as shown in Fig. 6(a). Such modification is generally inaccessible and may jeopardize the stability and reliability of CMOS process due to contamination and conformation issues. This work proposes to create the 10 μm thermal isolation cavity as shown in Fig. 6(b). The thermolegs are deposited and patterned by CMOS process. Post-process is then by vertical SiO_2 etching with the top aluminum layer as the etching mask to form the slit surrounding thermolegs, and similarly by isotropic Si etching to create the cavity beneath for thermal isolation. SiO_2 etching as shown in Fig. 6(c) is by inductive coupled plasma using C_4F_8 and incorporating O_2 for polymer formation on the sidewalls. Isotropic Si etching is by inductive reactive ion etching using SF_6.

Fig. 7(a) illustrates the layout of the 2000 μm × 2000 μm chip with generators in different thermoleg sizes as listed in Table 1. In view of the 4 μm etching window-limit in creating the cavity, the width of thermocouples is selected at 4 or 8 μm to ensure low contact resistance, complete etching, and high thermocouple density. Test structures are located around the perimeter for measuring the thermoelectric properties, and each test structure is a cantilever imbedded with different thermoelectric materials from the fixed to the free end. The 100 μm × 100 μm pads with 10 μm trenches around are fabricated by patterning the top metal layer M4 for electrical connection. Note that the generator chip with thermocouple length 20, 30, 40, 60, and 120 μm is fabricated before the analysis in Fig. 3. Interpolation is thus required, if applicable, to compare the analysis and measurement results.

The performance is characterized by 20 K temperature difference from a heating wire and commercial cold plate (thermoelectric cooler) as illustrated in Fig. 7(b). The μTEG chips are attached to a cold plate by thermal conductive gel, while a resistive hot wire is applied on the top surface of the chip. K_{int} is validated experimentally by curve fitting the simulation results from the thermal circuit model, and the result at about 9 cm^2K/W falls within the metal-ceramic interface of 1–20 cm^2K/W. The thermal resistance of a single optimal thermocouple 71 μm × 4 μm is 1.25×10^6 K/W from Eq. 1(b), and that of a 1 cm^2 μTEG containing 69,400 thermocouples is 18 K/W. This generator's thermal resistance is much higher than 1.555 K/W in Huesgen et al. [11] in which the poly-silicon thermocouple is 120 μm × 40 μm × 0.7 μm (length × width × thickness). For the design with wider W_g, the increase of a thermocouple unit area leads to smaller number of thermocouple N and hence lower output voltage, which is undesirable because of lower DC–DC converter efficiency in engineering applications. In view of the 4 μm constraint in dry etching window-limit, the optimal design is to have $L_g^* = 71$ μm and $W_g = 4$ μm for the maximum power 0.0473 μW/cm^2 K^2. In practice, the desired W_g is first selected by considering the CMOS fabrication constraints and the volatge/current output requirements, then the optimal length L_g^* is determined to maximize power, voltage, and current.

The output power and voltage shown in Table 1 are measured via the metal pads by the probe station (Wentworth Lab) and multimeter. Among the 10 thermocouple sizes, the set of 60 μm × 4 μm has the largest power factor 0.0417 μW/cm^2 K^2 and the voltage factor 2.417 V/cm^2 K, and they are comparable to the analysis of $L_g^* = 71$ μm, power factor 0.0473 μW/cm^2 K^2 and voltage factor 2.788 V/cm^2 K. This measument data is also compared with those reported in the literature. In Table 2, the first thin-film design was developed by Glosch et al. [7] in which the thermocouple of 500 μm × 7 μm can generate 0.091 μW/cm^2 K^2. Though having higher power factor, the membrane configuration of parallel thermal flow is impractical for on-chip thermal harvesting and it is not CMOS. A recent design using poly-SiGe with the power factor 0.0051 μW/cm^2 K^2 [9] and others using poly-silicon with 0.00137 μW/cm^2 K^2 [10] and with 0.00363 μW/cm^2 K^2 [11] are one order smaller than this work. Their fabrication process using wafer-bonding may also be unsuitable in batch production. The generator by Strasser et al. [8] has polycrystalline silicon and polycrystalline silicon germanium thin-film thermoleg of 18.5 μm × 6 μm and power factor 0.0426 μW/cm^2 K^2. Though the power factor is about the same as this work, their fabrication process requires a modified CMOS process for additional etching and thus may jeopardize the process stability. By comparison, the proposed design

is shown to have optimal size in delievering the power factor 0.0417 $\mu W/cm^2\,K^2$ and voltage factor 2.417 $V/cm^2\,K$. The fabrication process is CMOS compatible and suitable for engineering implementation.

5. Conclusions

(1) Applications of wireless sensor network (WSN) which consists of multiple wireless sensor nodes for sensing, computing, power managing, and communication are emerging. A recent study [15] indicated that a system-on-chip wireless sensor node with power requirement below 1 mW is possible. Today's software in a mesh network runs at about 1% radio duty cycle, and it is thus expected that the average node power consumption is of tens μW. Energy harvesting in this scale is applicable to low-frequency digital signal processor [16] and to MEMS devices with improving circuit, memory, and sensing [17]. The primary obstacle of micro thermoelectric generator design comes from its small thermal resistance. A generator is developed in this work, in which the heat input from the top surface is confined passing through in-plane thermolegs of optimal size. Thermal isolation design by a cavity beneath the thermocouples is applied to minimize heat leakage and facilitate better thermoelectric conversion. Analysis shows that the generator performance can be improved by higher temperature gradient across the thermocouples with thermal isolation cavity. A thermal circuit model is adopted to calculate the optimal thermocouple geometry at 71 μm in length, 4 μm in width, and 0.275/0.18 μm in thickness for P- and N-thermolegs in generating maximum power factor 0.0473 $\mu W/cm^2\,K^2$ and voltage factor 2.788 $V/cm^2\,K$.

(2) The design is validated by TSMC 0.35 μm CMOS process with two poly-silicon layers and four metal layers (2P4M) on a 2000 μm × 2000 μm chip. The patterned poly-silicon layers serve as the thermocouples, and they are interconnected by the aluminum pads to form the hot/cold junctions on an oxide layer. The aluminum layer also serves as the mask protecting thermocouples beneath in post-processing, and both vertical silicon dioxide etching and isotropic silicon etching in creating the thermal isolation cavity are conducted after all thin-film depositions to ensure process compatibility. The generator performance is characterized by 20 K temperature difference, and the measurement results show that, among the 10 lengths/widths, the thermoleg of 60 μm × 4 μm has the largest power factor 0.0417 $\mu W/cm^2\,K^2$ and voltage factor 2.417 $V/cm^2\,K$. Compared with the μTEGs of power factor 0.00363 $\mu W/cm^2\,K^2$ [11], 0.0051 $\mu W/cm^2\,K^2$ [9] and 0.00137 $\mu W/cm^2\,K^2$ [10], this design is one order higher in performance and is about the same as that in Strasser et al. [8]. All dry etchings are carried out after all thin-film depositions to ensure high yield in standard CMOS process.

(3) It should be noted that the measurement of the generator performance has always been troubled by the precise value of the interface thermal resistance K_{int} and by the experimental setup in maintaining constant temperature difference between the hot/cold sides. The value of the interface thermal resistance will affect the optimal length/width (thickness is determined by the standard CMOS process) of the thermolegs. In addition, the optimal size of thermolegs is also dependent upon the thermoelectric properties of the P- and N-thermolegs. These data for the thin-film structures in sub-micron range remain inconclusive in this study, and more samples are currently under investigation and will be reported.

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